Invited Paper

Engineering future light emitting diodes and photovoltaics with inexpensive materials: *Integrating ZnO and Si into GaN-based devices*

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ABSTRACT

Indium Gallium Nitride (InGaN) based PV have the best fit to the solar spectrum of any alloy system and emerging LED lighting based on InGaN technology and has the potential to reduce energy consumption by nearly one half while enabling significant carbon emission reduction. However, getting the maximum benefit from GaN diode -based PV and LEDs will require wide-scale adoption. A key bottleneck for this is the device cost, which is currently dominated by the substrate (i.e. sapphire) and the epitaxy (i.e. GaN).

This work investigates two schemes for reducing such costs. First, we investigated the integration of Zinc Oxide (ZnO) in InGaN-based diodes. (Successful growth of GaN on ZnO template layers (on sapphire) was illustrated. These templates can then be used as sacrificial release layers for chemical lift-off. Such an approach provides an alternative to laser lift-off for the transfer of GaN to substrates with a superior cost-performance profile, plus an added advantage of reclaiming the expensive single-crystal sapphire. It was also illustrated that substitution of low temperature n-type ZnO for n-GaN layers can combat indium leakage from InGaN quantum well active layers in inverted p-n junction structures. The ZnO overlayers can also double as transparent contacts with a nanostructured surface which enhances light in/out coupling. Thus ZnO was confirmed to be an effective GaN substitute which offers added flexibility in device design and can be used in order to simultaneously reduce the epitaxial cost and boost the device performance.

Second, we investigated the use of GaN templates on patterned Silicon (100) substrates for reduced substrate cost LED applications. Controlled local metal organic chemical vapor deposition epitaxy of cubic phase GaN with on-axis Si(100) substrates was illustrated. Scanning electron microscopy and transmission electron microscopy techniques were used to investigate uniformity and examine the defect structure in the GaN. Our results suggest that groove structures are very promising for controlled local epitaxy of cubic phase GaN.

Overall, it is concluded that there are significant opportunities for cost reduction in novel hybrid diodes based on ZnO-InGaN-Si hybridization.

Keywords: GaN, ZnO, Si, light emitting diode, photovoltaics, metal organic chemical vapor deposition, controlled local epitaxy, pulsed laser deposition

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1. INTRODUCTION

The growing world population and ever-increasing energy demands call for cheaper/renewable energy sources combined with energy savings in every aspect of our lives. With about 20% of annual energy being consumed for lighting (a $120 Billion industry with general lighting covering about 75% of it), environmental-friendly alternatives to existing lighting technologies are under investigation for energy savings. Photovoltaics (PV) and solid state lighting based on light emitting diodes (LEDs) are currently considered, respectively, the most promising technological candidates to provide sufficient renewable energy and dramatically reduce lighting energy consumption and related costs.

Gallium Nitride (GaN) technology offers unique opportunities for a whole range of applications for a number of reasons including: (1) GaN-based electronic devices (e.g. high electron mobility transistors) outperform those based on silicon and gallium arsenide in high power and high frequency regimes due to their combination of inherently high bandgap, critical electric field (~3.5 MV/cm) and saturation velocity (~2.5×10^7 cm/s) [1] (2) GaN photonics (e.g. LEDs, laser diodes (LDs) and PV) enable high efficiency deep ultraviolet (UV) to near-infrared devices due to their direct and tuneable bandgap [2]. However, without environmental-friendly and low-cost mass-production schemes, large scale adoption of GaN technology is unlikely and the technological benefits will be limited.

The recent upsurge in usage of GaN-based visible LEDs for general lighting applications has driven a huge worldwide demand for metalorganic chemical vapor deposition (MOCVD) of GaN. Despite such success, adoption of GaN LEDs for general lighting usage is currently hindered by the relatively high manufacturing costs [3]. A significant proportion of these costs is attributable to the epitaxial cost and the relatively expensive single crystal sapphire and silicon carbide substrates which are generally employed.

This paper discusses the advantages and challenges of integrating Zinc Oxide (ZnO) and Silicon (Si) into GaN-based devices so as to combat these issues. Since ZnO and Si, are composed of abundant and relatively inexpensive elements, they are promising candidates to use as substitutes for costly GaN epitaxy and sapphire/SiC substrates, respectively. Although such substitution may have potential to reduce the cost significantly, the engineering of hybrid devices comes with additional hurdles which necessitate new technological breakthroughs. This paper focus on engineering LEDs for solid state lighting and next generation PVs with such inexpensive materials and looks into novel concepts to overcome these hurdles.

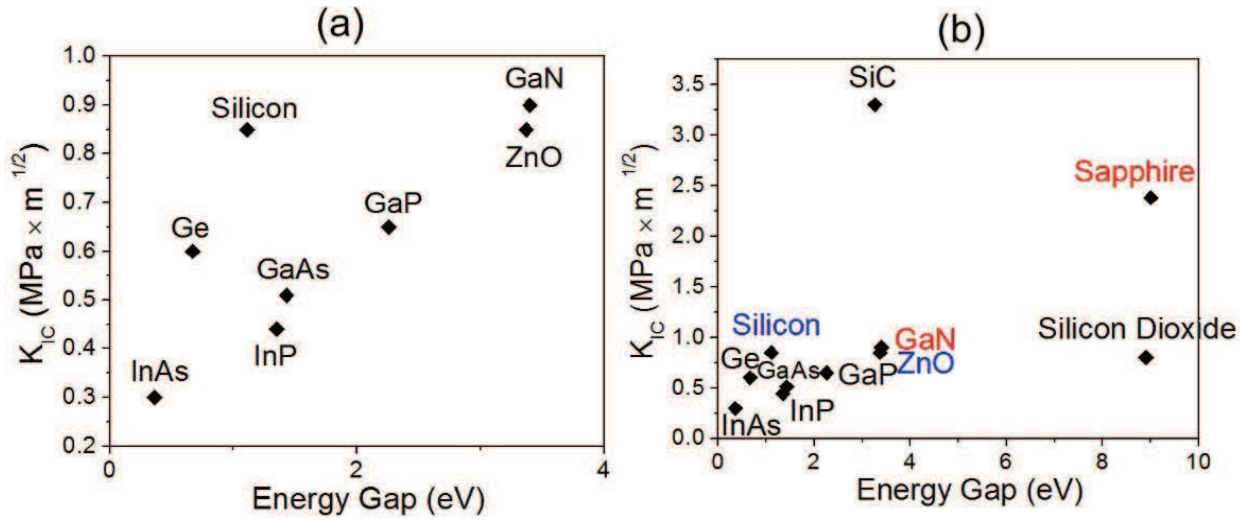

Figure 1. Fracture toughness K_{IC} of **(a)** Common materials and **(b)** Common materials with III-N substrates.

2. ZNO-INGAN HYBRIDIZATION

ZnO is a direct wide bandgap material (Eg=3.3 eV) with a relatively large exciton binding energy (60 meV). It also has a low toxicity, a highly tuneable conductivity (Al-doped ZnO is often adopted as a transparent electrode) and the same wurtzite structure as GaN. The small in-plane lattice mismatch (~1.8%) with GaN is often cited as making ZnO a good candidate for integration in nitride devices. [4,5] Recently, there have been many reports of UV emitters based on *n*-ZnO/*p*-GaN heterostructures. [6,7,8] Such devices benefit from the distinctive property set of ZnO, including the potential for strong excitonic emission. Moreover, the markedly increased susceptibility of ZnO to chemical dissolution (compared with GaN) opens up new opportunities for processing via wet etching. Indeed, this combination of a crystallograpic fit with GaN plus increased susceptibility to chemical etching, has led to ZnO being successfully employed recently as a sacrificial template underlayer for substrate release and GaN transfer to alternative substrates [9, 10]. Building on these possibilities, this paper further investigates the incorporation of ZnO as both an alternative buffer layer and a top contact epilayer for GaN technology.

2.1. Si as an alternative buffer

Conventional GaN-based devices employ III-Nitride-based buffer layers. These buffer layers are typically composed of binary GaN / AlN, ternary AlGaN or are formed via stacking a combination of such binary and ternary layers. Coming from the same material family, such buffers offer growth convenience combined with similar crystalline properties. III-V materials such as GaAs and InP, on the other hand, possess similar advantages with a unique difference: chemical volatility. This difference is employed for enabling thin film devices such as solar cells via epitaxial lift-off technique. In such an approach, P-based underlayers can be selectively etched, so as to release As-based epitaxial layers. For III-Nitrides, enabling such epitaxial release is not straightforward. Similar crystalline structure and lattice parameter for III-Nitride regrowth with different chemical volatility for release are the requirements. One alternative is to look to another material family: i.e. II-VI semiconductors. As well as the use of ZnO as a buffer for III-Nitride [11] silicon, a group IV element, is a promising alternative as a buffer, with its significant difference in chemical and mechanical toughness with respect to III-Nitrides[12].

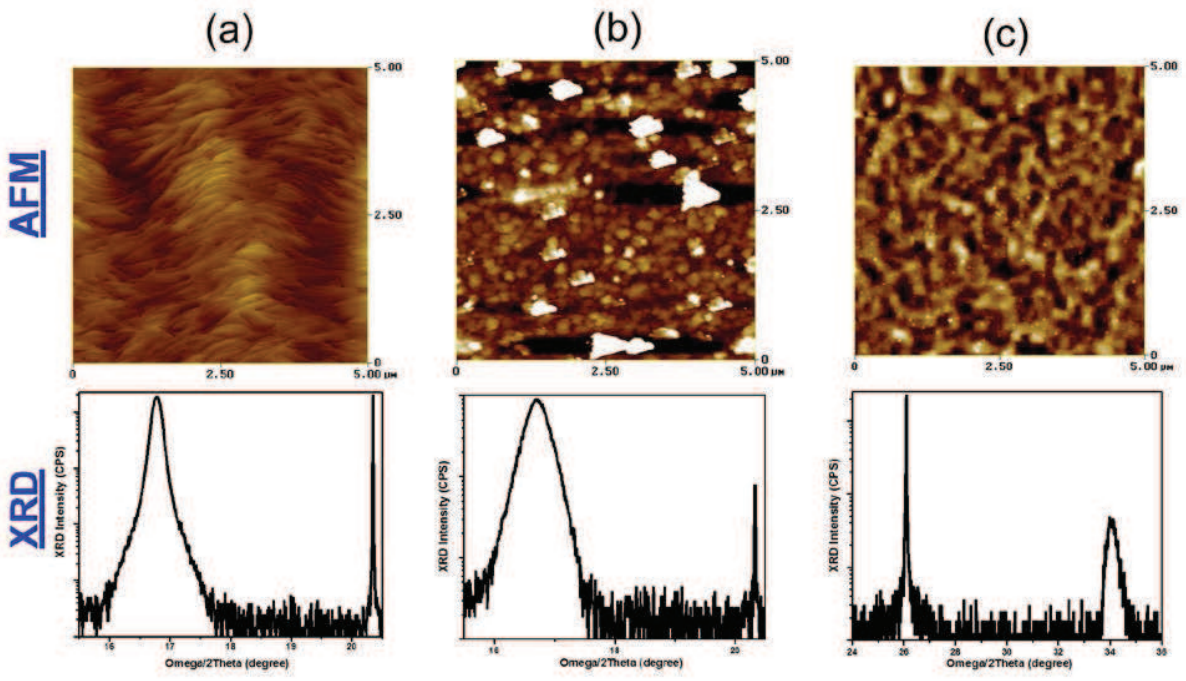

Figure 2. AFM images and Omega/2Theta XRD scans for **(a)** Conventional GaN on sapphire, **(b)** ZnO on sapphire, and **(c)** Silicon on sapphire. AFM RMS roughness is **(a)** 3.8, **(b)** 39.9, and **(c)** 1.6 Å.

2.1.1. Experiment

The chemical volatility of ZnO underlayers that enables release of III-Nitride layers poses a challenge during the growth of the III-Nitride layers. This is especially true for the MOCVD process, in which the growth typically employs gaseous phase reactants which etch away the ZnO. To investigate this problem, various buffer layers (GaN, ZnO, and Si - all on sapphire) were studied in order to establish the best case scenario(s).

2.1.2. Results and Discussion

We first characterized the morphological and crystalline properties of the various buffers: (a) conventional GaN on sapphire, (b) ZnO on c-sapphire and (c) silicon on sapphire. The atomic force microscope (AFM) revealed root mean square (RMS) roughnesses of **(a)** 3.8, **(b)** 39.9, and **(c)** 1.6 Å, as illustrated in **Figure 2**. The X-ray diffraction (XRD) omega/2theta scans show peaks for both the epilayer and the substrate for each combination. Although silicon on sapphire appears promising, such templates are relatively expensive and not widely available as they employ Si(100) on r-plane sapphire. In this respect, to begin with, we have focused our attention to ZnO on sapphire templates for enabling III-Nitride regrowth.

Figure 2 shows scanning electron micrographs (SEM) and omega/2Theta XRD scans for GaN grown on ZnO/sapphire templates under two different growth conditions: (a) Conventional and (b) Modified. The conventional growth process employed a H_2/N_2 mixture of carrier gas with ammonia (NH_3) flow during heat-up and nucleation. GaN regrowth temperatures from 700ºC to 1000ºC were employed. **Figure 3**(a) represents the best case outcome. In order to improve the surface morphology, N_2 carrier gas and a nucleation composed of prealuminization (supplying Trimethlyaluminum (TMAl) prior to any growth) were employed, followed by introducing NH_3 along with Trimethylgallium (TMGa) (i.e. no NH_3 supply beforehand) . This new approach improved both the morphology and the crystalline quality, as shown in **Figure 3** (b). However, there is still a lot of room for improvement. Going forward, it is envisaged that a protective layer be deposited on the ZnO surface prior to growth. This protective structure could be (Atomic Layer Deposition) ALD-deposited Al_2O_3, as when heated up it will be recrystallize and protect the underlying ZnO.

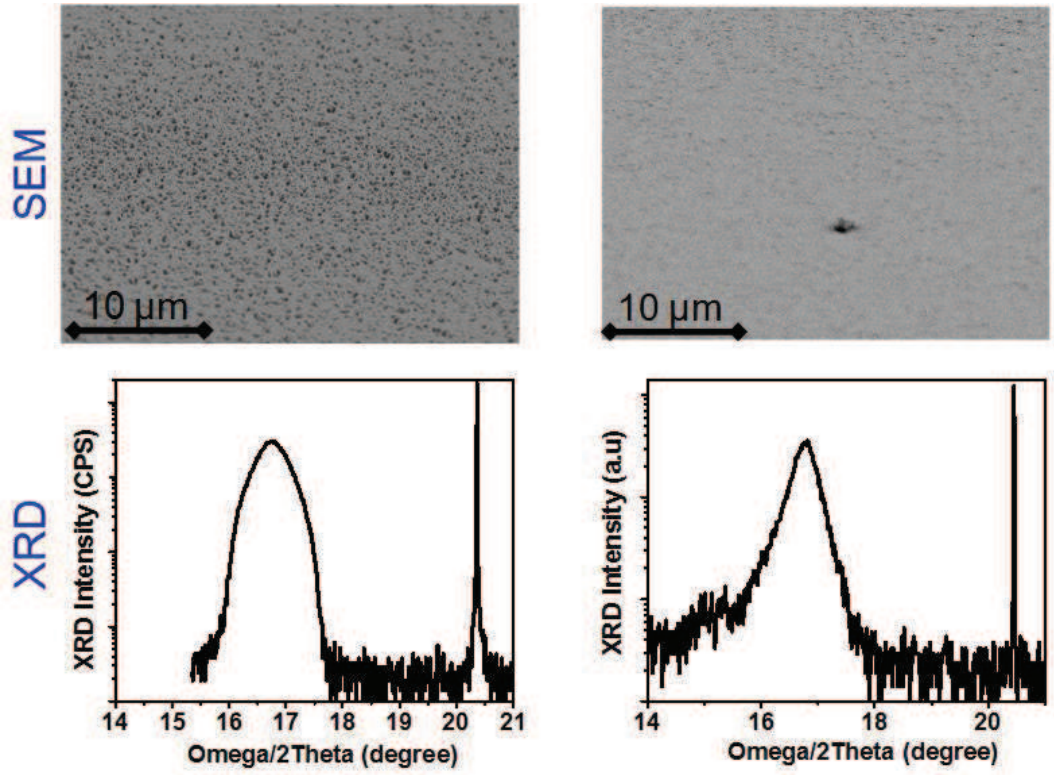

Figure 3. SEM and Omega/2Theta XRD of 400-nm-thick GaN deposited by MOCVD on ZnO/Sapphire under **(a)** Conventional growth process and **(b)** Modified growth process.

2.2. ZnO as an alternative contact epilayer

The higher In content required in the active layers for green LEDs and efficient GaN-based PV causes problems. Firstly, the limited solubility of In in GaN [13] imposes a restricted growth window for the InGaN active layer. Secondly, InGaN with high In content becomes unstable at elevated substrate temperature (Ts). [14] Conventionally, a *p*-GaN overlayer is grown on top of an InGaN multi-quantum-well (MQW) active layer. The *p*-GaN layer is grown at significantly higher Ts than the InGaN MQW active layer in order to obtain high structural quality. This leads, however, to indium leaking out of the active layers, which reduces the LED output (or PV efficiency). [15,14] Thus, it is important to combat In diffusion in order to obtain InGaN based PVs and green LEDs with superior performance.

In conventional GaN-based LEDs, the *p*-layer is deposited on top of the *n*-layer, because the *n*-layer can be grown with higher crystallographic and morphological quality than the *p*-layer. In previous work, we combated this by adopting an inverted LED structure employing an *n*-ZnO layer grown on top of (In)GaN MQW/*p*-GaN/AlN/Sapphire. [16,17,18,19]. Through the use of pulsed laser deposition (PLD), a high quality *n*-ZnO layer could be grown at significantly lower Ts than is typically required for GaN growth in MOCVD. This approach could be beneficial, particularly for green light emitters, in which, the high In content InGaN active layers are adversely affected by the high substrate temperature (Ts) required for the GaN growth. Furthermore, the refractive index of ZnO (at 500 nm) is 2.0 compared with 2.5 for GaN. Thus, lower critical angle loss is expected for light extraction through ZnO-capped LEDs, as shown in figure 4 [20].

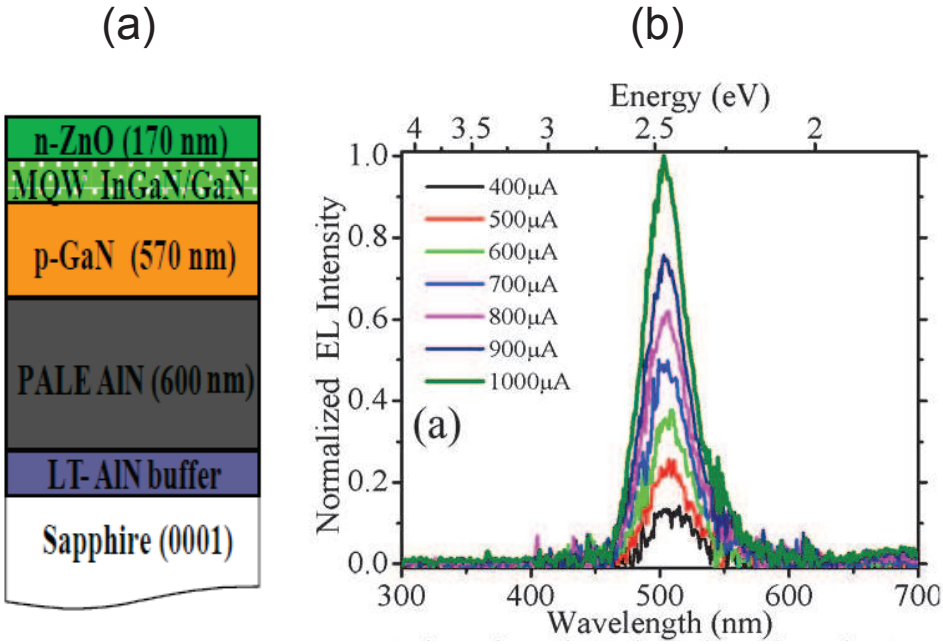

Figure 4. **a,** Schematic structure of a hybrid green LED. **b,** Normalized electroluminescence (EL) intensity of the hybrid green LED at room temperature.

Results and Discussion

Nanovation has recently developed know-how for self-forming surface nanostructuration of transparent conducting ZnO, which could enhance optical absorption for PVs and light extraction for LEDs and thus further boost overall efficiency. In typical PVs, ≥10% of incident light is lost through reflection if no anti-reflection (AR) measures are taken. Conventional AR coatings (typically thin film bilayers or surface roughening) usually only reduce the reflectance down to about 5-10%. To go beyond this, special surface treatments are needed. The vertically-aligned moth-eye–like nano-arrays developed by the Nanovation offer a much higher performance alternative.

Indeed, recent reflection studies showed < 0.5% of reflected light for all visible wavelengths over incidence angles up to 60° from the normal (**Figure 5**). This is probably due to the graded effective refractive index produced by the sub-optical tapering of the nanocones. Thus an improvement of overall efficiency is expected for PV & LEDs with such a surface

structuration. **Figure 5** shows a schematic of such a structure [21] and the SEM image of the surface of a first prototype. Furthemore, the self-forming ZnO AR nanostructuration can be made as a modification of the ZnO surface at minimal additional manufacturing cost (by simply changing the transparent conducting electrode layer growth conditions).

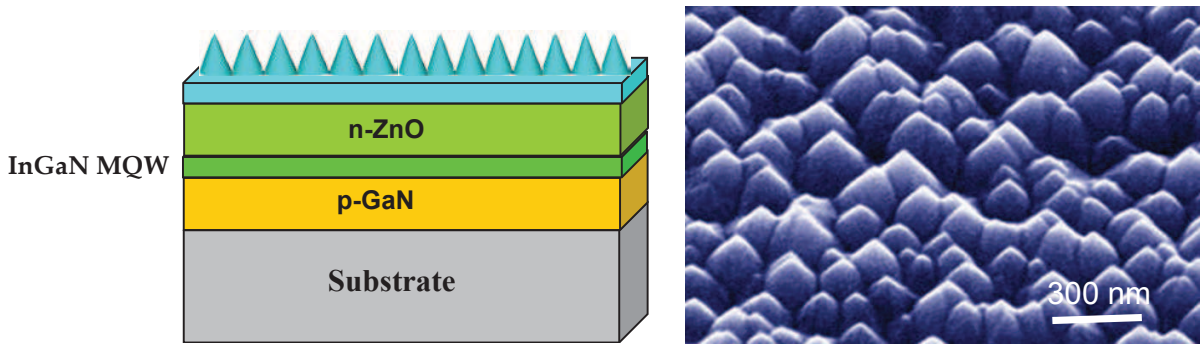

Figure 5. Illustration and SEM image of an inverted n-ZnO / InGaN MQW / p-GaN junction with a ZnO overlayer combining n-type, nano AR & transparent conductor functionalities.

Employment of ZnO on top of high indium content InGaN LEDs and PV could herald a new era of device designs as it solves the major problem of preventing the indium from leaking. Conventional LEDs employ a relatively thinner (~2 nm) InGaN well and thicker (~ 5nm) GaN barrier in order to stabilize indium content (and distribution) in the InGaN well. Indeed, the higher the desired wavelength, the higher the indium content and the thinner and thicker the well and barrier thicknesses, respectively. However, having such thin active layers when there are significant piezoelectric effects (due to the polar wurzite structure) lead to reduced recombination dynamics and carrier overflow phenomena under high injections. Thus, despite the increased power emission, the emission efficiency ("wall-plug efficiency") reduces under high injections. This phenomena is also known as efficiency droop. Besides, due to the temperature cycling required for conventional deposition of GaN-based contact layers, the indium segregation in the InGaN quantum wells is pronounced, which reduces the active area of emission significantly. Thus, conventional LED designs and approach are constrained by the reduce-to-practice requirements. In this respect, to fully eliminate efficiency droop, new approaches are essential.

Regarding the active layer, preventing efficiency droop for LEDs and capture efficiency for PV requires (1) minimized (if not eliminated) piezoelectric effects in the active layer and (2) a thick InGaN active layer with uniform indium distribution. In this respect, we are proposing new ZnO-InGaN concepts with low indium incorporation in quantum wells grown on non-polar substrates. This approach profits from semipolar structures which promise a higher rate of indium incorporation and significantly decreased piezoelectric fields. Furthermore, reduced defect density of freestanding substrates will enable a more uniform indium distribution as well more efficient radiative recombination.

Overall, combined with the semipolar freestanding GaN substrate, innovative ZnO – InGaN hybridization opens up perspectives for higher efficiency InGaN-based PV and green LEDs / LDs with superior spectral quality and thereby facilitates, for instance, better white LEDs based on color-mixing as well as more efficient projection TVs. Reduced costs by means of such a technology are also feasible through adoption of the cheaper source materials combined with emerging thin film growth techniques.

3. GAN-ON-SILICON TEMPLATES FOR LEDS

3.1. Silicon as an alternative substrate

Silicon could be an excellent low-cost alternative to sapphire and silicon carbide substrates for GaN LED volume production. Moreover, it is available in larger diameters and at relatively low cost. However, adoption of silicon as the GaN LED substrate requires overcoming the lattice-and thermal-mismatch (~17% and ~53%, respectively) issues which lead to defect densities of ~ 10^9 /cm^2 along with micro-cracks [1].

Conventional GaN growth on silicon utilizes a bulk deposition approach whereby a strain-engineered 2-3 μm buffer layer of $Al_XGa_{(1-X)}N$ is initially deposited to compensate for the thermal-mismatch with Si and yield higher quality GaN growth with better uniformity [22]. Current published research is focused mainly on blanket, or patterned, GaN (0001) (six fold) growth on (111) silicon [22]. However, successful growth of GaN on (001) silicon has many obvious benefits: (i) compatibility with existing Si Complementary Metal Oxide Semiconductor (CMOS) infrastructure in order to enable on-chip GaN-Si photonics and (ii) availability of industry-standard cleavage planes [1, 22]. However, anisotropic lattice-mismatch (i.e. ~ 14% $GaN<11\bar{2}0> \parallel Si<\bar{1}00>$ and ~0.6% for $GaN<10\bar{1}0> \parallel Si<\bar{1}00>$) [23] and crystallographic asymmetry (i.e. (wurtzite GaN) sixfold versus fourfold for (Si(001))) leads to GaN crystals with different rotations on the Si(001) surface, which results in twist boundaries and low quality epitaxy. Thus, offcut-oriented substrates (typically 4 to 7° towards (110)) are favored for single crystalline GaN epitaxy [24]. However, on-axis Si(001) is preferred in order to avoid any anisotropy and performance-related detrimental effects that may arise due to deviating from standard Si technology practices.[25].

In this work, GaN is grown on (100) Si by exposing {111} Si facets via lithographic patterning in conjunction with anisotropic etching (**Figure 6**) [26]. Dielectric trenches are patterned in aspect ratio trapping structures [27] - followed by selective etching of silicon in order to expose {111} Si facets at the bottom of trenches. The GaN hetero-epitaxial layers are subsequently grown selectively on the exposed silicon {111} facets. When the growth fronts meet, cubic face GaN emerges. These initial results show that polarization-free cubic phase GaN on Si (001) is achievable via optimized aspect ratio trapping structures and MOCVD growth conditions.

3.2. Substrate Preparation and Epitaxial Deposition

Figure 6 shows a schematic of the process flow for silicon (001) substrate preparation prior to MOCVD growth in an AIXTRON reactor. First, CMOS-compatible Si (001) is cleaned via a standard Radio Corporation of America (RCA) process. Then, a 500-nm-thick thermal oxide (SiO_2) is grown, followed by deep ultraviolet (193 nm) lithography and reactive ion etching. After another RCA-like cleaning process, the wafer is submerged in KOH (10%) solution so as to selectively etch the Si and expose the {111} facet family at the bottom of the trench (**Figure 6**e, SEM). Once the desired groove shape is formed, the native oxide at the bottom of the trench and surrounding regions is removed in dilute HF prior to GaN growth.

TMAl and TMGa were used as the epi sources for Al and Ga, respectively. NH_3 and H_2 were used as the anion source and carrier gas, respectively. SEM and transmission electron microscopy (TEM) were used to determine the uniformity and quality of the patterned GaN.

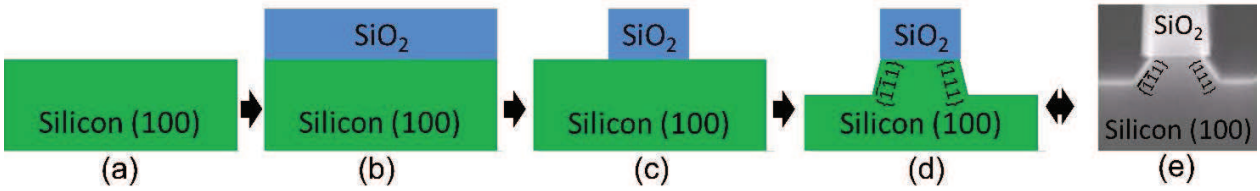

Figure 6. Schematic process flow of silicon (001) substrate preparation for MOCVD growth. a, RCA cleaning of Silicon (100) substrate. **b,** Thermal oxide (SiO_2) growth on Silicon (100). **c,** Deep UV (193 nm) lithography and reactive ion etching of oxide (SiO_2). **d,** Selective etching of parent Silicon (100) substrate and formation of the {111} family of planes. **e,** SEM image of an actual structure corresponding to sketch **d**.

MOCVD regrowth of GaN on patterned Si (100) was realized as follows: (1) removal of any native oxide, (2) aluminization of the Si surface, (3) AlN buffer deposition, and (4) GaN growth at > 950 °C. For GaN growth on the AlN buffer, TMGa and NH_3 were supplied together in a conventional manner. Higher temperature regrowth of GaN acts for annealing the AlN buffer, improving and providing sites for, GaN nucleation. Such nucleation should be more pronounced on Si {111} facets than on Si {001} as the former has the same symmetry as GaN. Moreover, higher temperatures increase Ga adatom mobility, leading to better site selection.

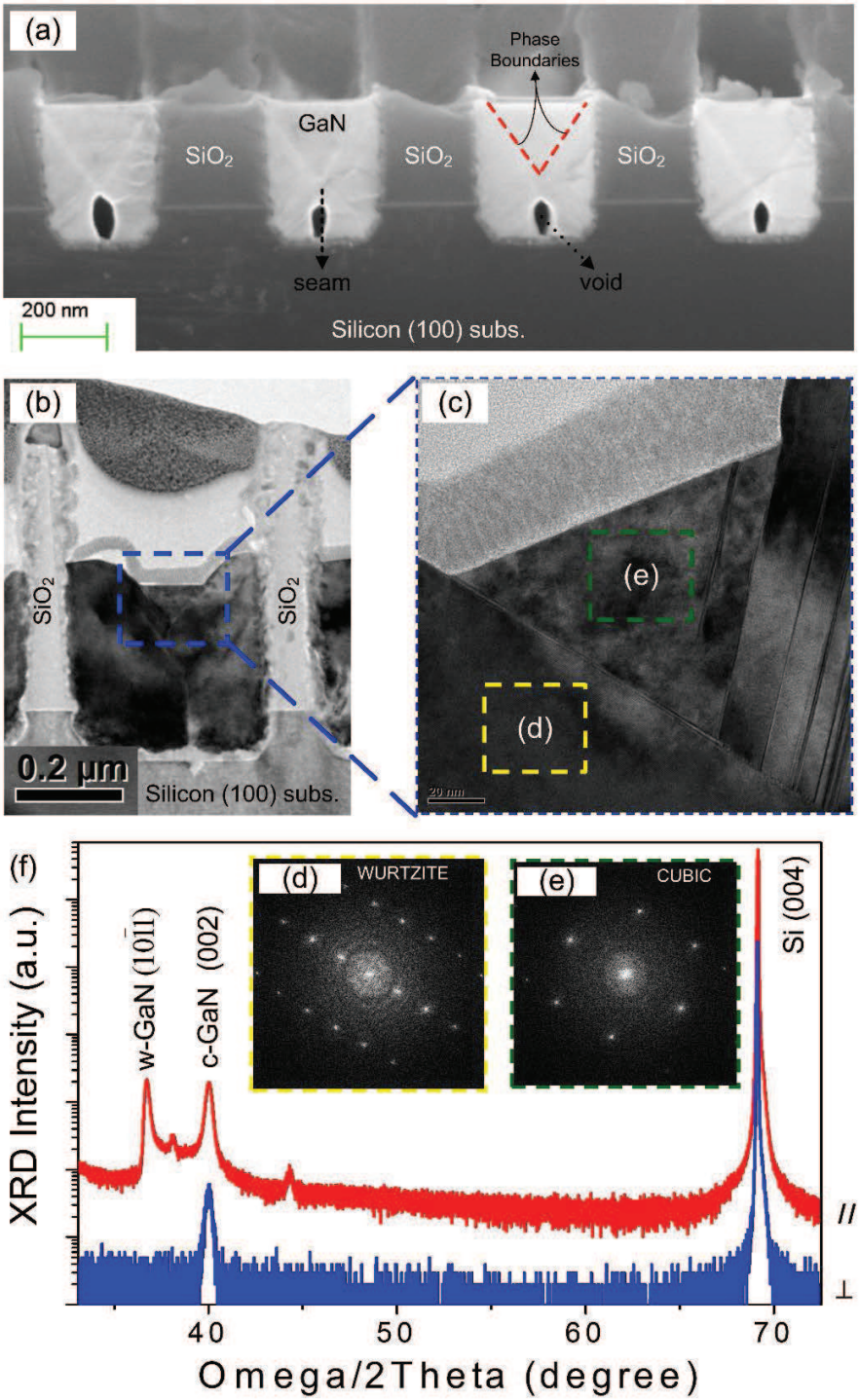

Figure 7. **(a)** Cross-sectional SEM of GaN grown on a nanopatterned Si (100) substrate, **(b)** Cross-sectional bright-field TEM of GaN partially-filled in one period of a [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structure (period is 250 nm), **(c)** Cross-sectional bright-field TEM image of the zoomed-in seam area, **(d,e)** Selected area electron diffraction pattern of regions (d,e) shown in (c) generated by FFT, **(f)** Omega/2Theta XRD scans of GaN film grown atop a nanopatterned Si (100) substrate. XRD scans performed paralell (//) and vertical ($\perp$) to the nanopattern direction.

3.3. Results and Analyses

GaN growth studies were conducted on [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structures (**Figure 7**) by MOCVD. Short period groove structures are of particular interest to increase effective GaN epitaxial coverage on Si (100) substrates without increasing the epitaxial deposition time. **Figure 7** shows GaN filled in such grooves (of 250-nm period). Interestingly, **Figure 7**(a) highlights two distinct features: voids and crystallographic faults emanating from the seam.

In such groove structures, GaN growth nucleates predominantly on the Si {111} family facets. The [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structures have two nucleation sites for GaN: Si (111) and Si $(\bar{1}\bar{1}\bar{1})$ surfaces. When the GaN lateral growth fronts meet, a void is formed approximately in the middle, where the seam is expected (**Figure 7**(a)). The formation of the void depends on the groove period as well as the growth parameters [28].

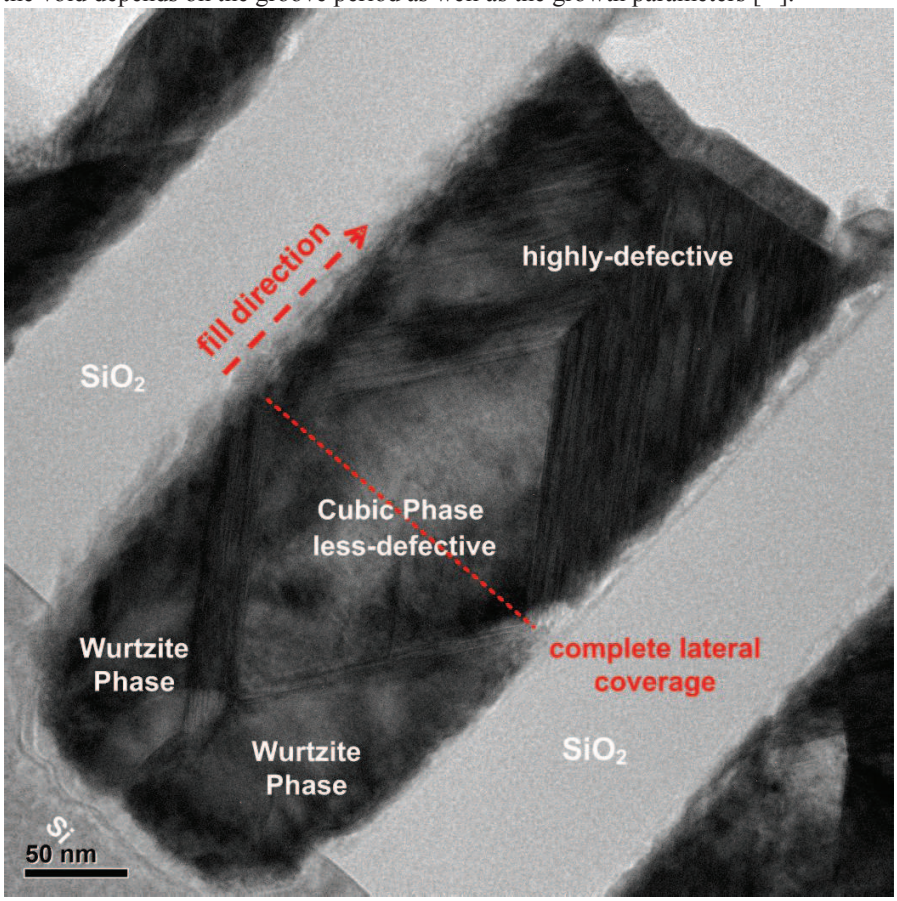

Figure 8. Cross-sectional TEM of GaN filling in one period of [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structure (period is 250 nm). GaN defectivity and phase are highlighted in text.

The second distinct feature, crystallographic faults initiated at the seam are further investigated by TEM. **Figure 7**(b) shows the bright-field TEM of a single period groove structure. Clear crystallographic faults are observed by TEM in the seam area. **Figure 7**(c) shows a bright-field TEM image, zoomed in on the seam area, highlighting the crystallographic faults. In order to understand the GaN crystalline phase below and above the crystallographic faults, electron diffraction patterns of regions inside the rectangular areas were examined (shown in **Figure 7**(c)) - regions (d) and (e) being below and above the crystallographic faults, respectively - are generated by fast Fourier transform (FFT). The resulting diffraction patterns are shown in **Figure 7**(d) and (e). These correspond to different crystallographic phases: wurtzite and cubic, respectively [29, 30]. Such a phase transition indicates that the crystal faults observed at seam delineate phase boundaries where wurtzite GaN (w-GaN) becomes cubic GaN (c-GaN). Moreover, the V-shape form of the phase

boundaries helps suppress threading dislocations in the cubic GaN, as the newly-formed cubic phase growth front is aligned with the Si[100] direction rather than the wurtzite phase growth front: w-GaN $(000\bar{1})$.

XRD studies were carried out to investigate the two different phases of GaN. **Figure 7**(f) plots the Omega/2Theta XRD data taken parallel (//) and vertical ($\perp$) to the pattern direction. Both scans revealed a peak at ~40° corresponding to cubic c-GaN (002). Interestingly, the vertical ($\perp$) scan revealed an additional peak at ~37° which corresponds to the w-GaN $(10\bar{1}1)$ plane. Two other weaker peaks at ~38° and ~44° were observed but only when the w-GaN $(10\bar{1}1)$ peak was present and not during the parallel (//) scan. This is most likely due to the six-fold symmetry of w-GaN such that tilting by 90° misaligns any w-GaN plane diffraction condition. It is also important to note that as c-direction of the w-GaN is aligned with the Si<111> direction, there is a significant tilt of the planes with respect to the Si (100) planes. In summary, it was demonstrated that during GaN regrowth a phase change can be induced through use of [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structures on a Si (100) substrate. Such a wurtzite to cubic phase transition could be particularly beneficial for LEDs since the cubic phase is non-polar which eliminates piezoelectric fields and enhances radiative recombination dynamics.

Figure 8 shows a TEM image of GaN grown after the phase transition occurs. Almost complete coverage of the groove is realized. As GaN fills the groove further than the complete lateral coverage, it would appear that nucleation starts from the sidewalls as well. This might be because the AlN low temperature buffer is deposited everywhere and can act as a nucleation site where the competition plane is cubic phase GaN at high growth temperature. As such, a highly-defective GaN layer then grows on top. This shows that the oxide mask thickness and the [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structure needs to be predesigned for the targeted end application. Our results indicate that an oxide thickness of 150 nm is enough to enable complete coverage of cubic phase GaN for an opening of 200nm and a Si etch depth of 50 nm.

In order to demonstrate visible luminescence, InGaN/GaN multi-quantum-well structures were grown on cubic phase GaN on silicon templates. **Figure 9** shows the room temperature photoluminescence revealing contributions from the GaN in the UV range and the InGaN/GaN MQW in the blue range This suggests that such templates can be an attractive alternative to existing substrates. The cubic nature of the GaN surface, in particular, is of importance, as the GaN overlayer should also be cubic in nature – i.e. no piezoelectric effects are expected.

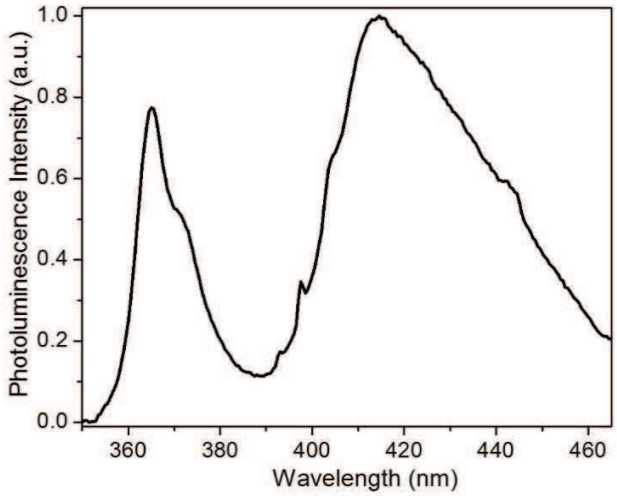

Figure 9. Room-temperature photoluminescence spectrum for an InGaN/GaN multi-quantum-well grown on a [SiO_2-Si{111}-Si{100}-Si{111}-SiO_2] groove structure (period of 250 nm). UV and blue luminescence are observed from the GaN and QWs, respectively.

4. CONCLUSION

ZnO and Si are both relatively inexpensive and abundant materials. This makes them attractive substitutes for more expensive/rare elements/compounds such as In, Ga, SiC and sapphire in InGaN-based LEDs and PVs. This paper, first of all, illustrated the successful MOCVD regrowth of GaN on ZnO thin film templates, which can then be used as sacrificial release layers for chemical lift-off. Such an approach provides an alternative to laser lift-off for the transfer of GaN to substrates with a superior cost-performance profile, plus an added advantage of reclaiming the expensive single-crystal sapphire. Next, it was illustrated how n-type ZnO, grown at relatively low temperatures, can be a good replacement for the n-type GaN layer in inverted LED and PV structures. Such, an approach could be particularly pertinent for high indium content (green) emitters (and sweet spot PV) by combating the effects of indium leaking from the active layers and thereby degrading the optical and electrical performance. It is also projected than maintaining the integrity of the InGaN (combined with the use of non-polar layers) could reduce the problem of LED droop. A further strong point of the n-type ZnO overlayer was illustrated: the capacity to tune the conductivity and surface morphology via the growth conditions so as to have a transparent conductor surface with a nanostructured texture that dramatically enhances optical in/out-coupling.

Nanopatterned, high aspect ratio, groove structures on Si (100) substrates were demonstrated to increase GaN epitaxial coverage and generate excellent GaN-on-Si templates. Cubic phase GaN formation was identified using electron diffraction and verified by XRD studies. Further TEM studies identified a GaN phase transition from wurtzite to cubic at seams and threading dislocations which were partially filtered by phase boundaries. Overall, a unique epitaxial integration scheme for GaN on Si(100) substrates was demonstrated that is CMOS-compatible and mass reproducible.

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